REMARKS

Claims 1 and 3-20 are all the claims presently pending in the application. Claims 1 and 20 have been amended to clarify the invention. Claims 3-19 have been withdrawn from prosecution. Of the remaining claims, claims 1 and 20 are independent.

These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Applicants also note that, notwithstanding any claim amendments herein or later during prosecution, Applicants' intent is to encompass equivalents of all claim elements.

Entry of this §1.116 Amendment is proper. Since the Amendments above narrow the issues for appeal and since such features and their distinctions over the prior art of record were discussed earlier, such amendments do not raise a new issue requiring a further search and/or consideration by the Examiner. As such, entry of this Amendment is believed proper and Applicants earnestly solicit entry. No new matter has been added.

Claims 1 and 20 stand rejected under 35 U.S.C. § 112, second paragraph and under 35 U.S.C. § 103(a) as being unpatentable over Houlihan, et al. (U.S. Patent No. 6,258,673 B1) in view of Campardo, et al. (U.S. Patent No. 6,060,753).

This rejection is respectfully traversed in the following discussion.

I. THE RESTRICTION REQUIREMENT

The Office Action withdraws claims 3-19 from prosecution as allegedly being directed to an invention which is independent or distinct from the invention which was originally claimed because: "claims 3-19 could be made by a process materially different

from those/that of claims 1-2."

Applicants respectfully traverse this restriction requirement.

The remarks of the Amendment that was filed on August 20, 2003 pointed out that the Examiner's restriction requirement was prima facie insufficient because of the failure to show a serious burden on the Examiner to search and examine the claims of the entire application in accordance with the requirements set forth in § 803 of the M.P.E.P.

In response, the Examiner appears to attempt to allege that a serious burden is established because "a method for fabricating on a semiconductor device requires a different field of search and a different thought process."

Again, the Examiner completely ignores the specific requirements that are clearly set forth in § 803 of the M.P.E.P. that the Examiner is required to show before the Examiner is able to allege a prima facie showing of a serious burden.

> "For purposes of the initial requirement, a serious burden on the examiner may be *prima facie* shown if the examiner shows by appropriate explanation of separate classification, or separate status in the art, or a different field of search as defined in MPEP § 808.02" (emphasis added, M.P.E.P. § 803).

The Examiner has failed to even meet, in the words of the M.P.E.P., the initial requirement for a *prima facie* showing of a serious burden.

> "The examiner, in order to establish reasons for insisting upon restriction, must show by appropriate explanation one of the following:
>
> (A) **Separate classification thereof**: . . .
>
> (B) **A separate status in the art when they are classifiable together**:

. . .

(C) **A different field of search**: Where it is necessary to search for one of the distinct subjects in places where no pertinent art to the other subject exists, a different field of search is shown, even though the two are classified together. The indicated different field of search must in fact be pertinent to the type of subject matter covered by the claims. Patents need not be cited to show different fields of search.

Where, however, the classification is the same and the field of search is the same and there is no clear indication of separate future classification and field of search, no reasons exist for dividing among related inventions."

(Emphasis original, M.P.E.P. § 808.02)

In this instance, the Examiner is clearly alleging a "different field of search." However, the Examiner has failed to meet the minimum requirements by failing to provide "an appropriate explanation" that "it is necessary to search for one of the distinct subjects in places where no pertinent art to the other subject exists" as required by M.P.E.P. § 808.02.

Rather, the Examiner completely ignores and indeed, continues to flout the clear requirements of the M.P.E.P., by merely summarily alleging that the withdrawn claims require a "different field of search" without any attempt at all at providing any explanation at all, let alone an "appropriate explanation" that "it is necessary to search for one of the distinct subjects in places where no pertinent art to the other subject exists" as is clearly required by M.P.E.P. § 808.02 This is *prima facie* reversible error.

Regarding, the Examiner's allegation that the withdrawn claims require "a different thought process," places a serious burden on the Examiner. Applicant respectfully points out

that "different thought processes" are not available to the Examiner as a reason to allege a serious burden. Nowhere within the M.P.E.P. is there any reference to any differences in thought processes as having any bearing on whether there is a serious burden to search and examine the withdrawn claims.

The Examiner also continues to ignore that the process of making which is recited in claims 3-19 have already been searched and examined as evidenced by the Office Action issued on February 27, 2002. Therefore, there can be no serious burden to examine these claims. This invention has already been examined. Therefore, there clearly is no serious burden to the Examiner.

The Examiner asserts in the January 29, 2003 Office Action that the February 27, 2002 Office Action indicated that claims 3-17 was not searched. Contrary to the Examiner's assertion, not only does the February 27, 2002 Office Action not indicate that claims 3-17 was not searched, but that Office Action rejected those claims under 35 U.S.C. § 103(a) as being unpatentable over Shimizu et al. in view of Huang et al. Therefore, the Examiner's assertion that these claims were never searched is completely false because those claims must have been search in order to reject these claims.

Indeed, the Examiner does not contradict these facts in the May 20, 2003 and November 18, 2003 Office Actions.

Rather, the Examiner chooses to continue to ignore the fact that the Examiner has already searched these claims and does not make any attempt to address this fact in the November 18, 2003 Office Action.

Applicants respectfully submit that the subject matter of all claims 1 and 3-20 is sufficiently related that a thorough search for the subject matter of any one group of claims

would necessarily encompass a search for the subject matter of the remaining claims. Thus, Applicants respectfully submit that the search and examination of the entire application could be performed without serious burden.

M.P.E.P. § 803 clearly states that "if the search and examination of the entire application can be made without serious burden, the Examiner must examine it on its merits, even though it includes claims to distinct or independent inventions" (emphasis added). Applicants respectfully submit that the Examiner has clearly failed to provide a prima facie showing of a serious burden by failing to provide "by appropriate explanation of separate classification, or separate status in the art, or a different field of search" (M.P.E.P. § 803).

Applicants respectfully submit that the policy requiring examination of an entire application even though the Examiner alleges that it may include distinct inventions, should be applied in the present application in order to avoid unnecessary delay and expense to Applicants and duplicative examination by the Patent Office. Applicants respectfully request reconsideration and withdrawal of the restriction requirement and to examine all claims in this application.

Applicants respectfully request withdrawal of the restriction requirement and/or rejoinder of claims 3-19.

II. THE CLAIMED INVENTION

A first exemplary embodiment of the claimed invention is directed to a semiconductor device that includes a first MOSFET having a first gate oxide film, a second MOSFET having a second gate oxide film that is thicker than the first gate oxide film, and a third MOSFET of a p-type having a third gate oxide film which is thicker than the first gate oxide film and is

thinner than the second gate oxide film. The second MOSFET and the third MOSFET form a single CMOS pair.

A second exemplary embodiment of the claimed invention is directed to a semiconductor device which includes a semiconductor device comprising a first MOSFET, a second MOSFET and a third MOSFET. The first MOSFET has a relatively low threshold level and a first gate oxide film. The second MOSFET is an n-type with a relatively higher threshold level than the first MOSFET and a second gate oxide which is thicker than the first gate oxide film. The third MOSFET is a p-type with a relatively higher threshold level than the first MOSFET and a third gate oxide film that is thicker than the first gate oxide film and thinner than the second gate oxide film. Implantation treatments of fluoride ions in the regions of the high threshold level MOSFETs are performed before forming the gate oxide films. The fluoride ions encourage the oxidation of the gate oxide films. Each implantation is different for the high threshold level MOSFETs. The second MOSFET and the third MOSFET form a single CMOS pair.

A third exemplary embodiment of the present invention is directed to a method for fabricating a semiconductor device on a semiconductor substrate. The method includes forming an isolation region within a semiconductor substrate and close to a surface of the semiconductor substrate to define a first region for a first gate oxide film of a first MOSFET and a second region for second and third MOSFETs. The method also includes selectively implanting fluorine ions into a first part of the second region with a first ion-implantation condition. The first part of the second region is for the second MOSFET. The first ion-implantation condition is determined to form a second gate oxide film.

The method also includes selectively implanting fluorine ions into a second part of the

second region with a second ion-implantation condition. The second part of the second region is for the third MOSFET. The second ion-implantation condition is determined to form a third gate oxide film. The method also includes simultaneously growing oxide films on and over the first and second regions of the semiconductor substrate and forming the first to third MOSFETs by using the simultaneously grown oxide films, so that the first to third MOSFETs have the first to third gate oxide films, respectively. The second gate oxide film is thicker than the first gate oxide film and the third gate oxide film is thicker than the first gate oxide film and is thinner than the second gate oxide film.

Additionally, the threshold level of the first MOSFET is relatively low and the threshold levels of the second and third MOSFETs are relatively high, and the second MOSFET is an n-type and the third MOSFET is a p-type. This method provides a single CMOS pair with the second MOSFET and the third MOSFET.

Conventional processes for fabricating semiconductor devices with MOSFETs having different threshold levels use selective implantation of fluorine ions to provide gate oxide films having different thicknesses. However, these methods have never been applied to CMOS circuit fabrication which takes into consideration the properties of n-type and p-type MOSFETs into a single CMOS pair.

By contrast, the present invention is a configuration and method which provides a single CMOS pair which can achieve high speed operation, high reliability and low consumption power using suitable gate oxide film thicknesses. This is a non-trivial matter because, as the inventors discovered, n-type and p-type MOSFETs operating with the same threshold level have gate-channel leakage current characteristics which are different from each other.

Thus, the inventors discovered that the thickness of the gate oxide film of the p-type MOSFET does not need to be equal to that of the n-type MOSFET. To the contrary, the inventors discovered that the thickness of the gate oxide film of the p-type MOSFET may be thinner than that of the complimentary n-type MOSFET in a single CMOS pair because the leakage current of the p-type MOSFET is one order of magnitude smaller than that of the n-type MOSFET. Additionally, the thinner gate oxide film of the p-type MOSFET increases the operating speed.

III. THE PRIOR ART REJECTION

The Examiner alleges that the Campardo et al. reference would have been combined with the Houlihan et al. reference to form the claimed invention. Applicants submit, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Firstly, Applicants submit that these references would not have been combined as alleged by the Examiner. Indeed, the references are directed to completely different matters and problems.

Specifically, the Houlihan et al. reference is directed to avoiding the pitfalls of a first conventional method of requiring multiple HF etches (col. 1, lines 18-25) and a second conventional method of relying solely upon nitrogen implantation (col. 1, lines 26-32) to provide different gate oxide film thicknesses for generic transistors by combining aspects of each of these conventional methods (col. 2, lines 11-57).

In contrast, the Campardo et al. reference is specifically directed to solving the "problems which are encountered when an output stage of an electronic circuit is required to

change its logic output value." (col. 1, lines 58-60). The Campardo et al. reference addresses this problem by providing a pull-down transistor with a three-well design (col. 5, lines 29-30) so that voltage variations at the ground terminal of the output buffer will not reflect on the internal ground terminal of the input buffer (col. 5, lines 49-53).

One of ordinary skill in the art would not have been motivated to modify the disclosure of the Houlihan et al. reference based upon the teachings of the Campardo et al. reference because the Campardo et al. reference is not directed to avoiding the pitfalls of a first conventional method of requiring multiple HF etches and a second conventional method of relying solely upon nitrogen implantation with which the Houlihan et al. reference is concerned. Rather, the Campardo et al. reference is directed to the entirely unrelated and completely different problems which are encountered when an output stage of an electronic circuit is required to change its logic output value. Thus, these references would not have been combined, absent hindsight.

Further, Applicants submit that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner.

The Examiner alleges that it would have been obvious to one of ordinary skill in the art to modify the disclosure of the Houlihan et al. reference to provide a third MOSFET of p-type conductivity and a single CMOS pair "to provide a low-noise output stage for an electronic circuit integrated on a semiconductor substrate." However, the Campardo et al. reference does not teach or suggest that a single CMOS device provides a low-noise output stage.

Rather, the Campardo et al. reference teaches providing a low-noise output stage by providing a pull-down transistor with a three-well design (col. 5, lines 29-30) so that voltage

variations at the ground terminal of the output buffer will not reflect on the internal ground terminal of the input buffer (col. 5, lines 49-53). The Campardo et al. reference does not teach or suggest anything at all relating gate oxide thicknesses to anything at all, let alone relating a single CMOS device having different gate thicknesses to the ability to provide a low-noise output stage. Therefore, the Examiner's alleged motivation has absolutely nothing to do with gate oxide thicknesses.

The Examiner alleges that it would have been obvious to modify the teachings of the Houlihan et al. reference to incorporate the single CMOS pair disclosed by the Compardo et al. reference to one of ordinary skill in the art. The Examiner alleges that the motivation for making this modification is "to provide a low-noise output stage for an electronic circuit integrated on a semiconductor circuit." However, contrary to the Examiner's allegations, while the purpose of the Compardo et al. reference is to provide a low-noise output stage, the Compardo et al. reference does not teach or suggest that a single CMOS pair is what would provide a low-noise output stage, let alone disclose a single CMOS pair with transistors that have different gate oxide thicknesses.

The Compardo et al. reference explains that many electronic circuits have output stages which incorporate a complementary pair of transistors that forms essentially a CMOS inverter (col. 1, line 66 - col. 2, line 4). Thus, the Compardo et al. reference explains that CMOS pairs exist in the prior art and that these circuits are subject to the problems that the Compardo et al. reference is attempting to solve.

Therefore, contrary to the Examiner's allegation, the Examiner's alleged motivation has absolutely nothing to do with the presence of a single CMOS pair, let alone a single CMOS pair with transistors that have different gate oxide thicknesses.

Rather, as explained above, the Compardo et al. reference teaches that the purpose of providing a low-noise output stage is accomplished by providing a pull-down transistor with a three-well design (col. 5, lines 29-30) so that voltage variations at the ground terminal of the output buffer will not reflect on the internal ground terminal of the input buffer (col. 5, lines 49-53).

The disclosure of the CMOS pairs being present in the prior art of the Compardo et al. reference proves that a CMOS pair has absolutely no effect on the ability to "provide a low-noise output stage." Therefore, the Examiner's alleged motivation is completely irrelevant and inapplicable to the Examiner's alleged modification of providing a single CMOS pair to the Houlihan et al. reference.

Further, in the Response to Arguments section of the November 18, 2003 Office Action, the Examiner alleges that "utilizing the different gate oxide thickness of Houlihan et al. (sic) and the CMOS pair structure of Compardo et al. (sic) with the benefit of preventing of propagation of discharge current would have been obvious to one of ordinary skill in the art."

However, this statement by the Examiner provides evidence of a clear misunderstanding by the Examiner of the teachings of the applied references.

The Examiner alleges that it would have been obvious to combine the teachings of the different gate oxide thicknesses that are disclosed by the Houlihan et al. reference with the CMOS pair structure teaching of the Compardo et al. reference because the CMOS pair structure provides the "benefit of preventing propagation discharge current." However, contrary to the allegation, the prevention of a propagation discharge current has absolutely nothing to do with the presence of a CMOS pair.

Rather, as explained above, the Compardo et al. reference explains that prior art devices have included CMOS devices and have been subject to the problems of discharge current propagation.

Indeed, the Examiner's own citation of the abstract of the Compardo et al. reference makes it very clear that it is "The pull-down transistor [being] formed in a three-well structure [that prevents] propagation of a discharge current from the external load through the semiconductor substrate.

Therefore, contrary to the Examiner's allegation one of ordinary skill in the art would not have been motivated to modify the teachings of the Houlihan et al. reference to provide a CMOS pair to prevent propagation of discharge current because the Compardo et al. reference explains that the CMOS pair has absolutely no effect on the propagation of discharge current. Rather, the prevention of propagation of discharge current can only be achieved by providing a pull-down transistor formed in a three-well structure.

Moreover, even assuming arguendo that one of ordinary skill in the art would have been motivated to combine these references, the combination would not teach or suggest each and every element of the claimed invention.

The Examiner appears to be ignoring an important feature of the claimed invention. The claims do not merely recite a single CMOS pair. Nor do the claims merely recite transistors having different gate oxide thicknesses. Rather, the claims recite that a single CMOS pair has transistors that have different gate oxide thicknesses.

While the Houlihan et al. reference appears to disclose transistors having different gate oxide thicknesses, these transistors are merely on the same substrate. The Houlihan et al. reference does not teach or suggest providing a CMOS pair with transistors having different

gate oxide thicknesses.

In the Response to Arguments section of the November 18, 2003 Office Action, the Examiner alleges that "Houlihan et al. (sic) and Compardo et al. (sic) both teach CMOS (col. 2, lines 21-25 and abstract, respectively)." However, contrary to the Examiner's allegation, the Houlihan et al. reference does not teach or suggest a CMOS pair of transistors.

The Examiner's citation to col. 2, lines 21-25 of the Houlihan et al. reference does not mention anything at all regarding a CMOS pair of transistors. Rather, this portion of the Houlihan et al. reference is only discusses the preparation of the gate oxides and the preparation of the substrate 10 shown in Fig. 4.

Further, while the Compardo et al. reference appears to disclose CMOS pairs. The Compardo et al. reference, not only does not provide any motivation to modify anything to include CMOS pairs, but also fails to teach or suggest a single CMOS pair having transistors with different gate oxide thicknesses.

The applied references do not teach or suggest a single CMOS device with transistors that have different gate oxide thicknesses. As explained above, this feature is important for achieving high speed operation, high reliability and low consumption power using suitable gate oxide film thicknesses. This is a non-trivial matter because, as the inventors discovered, n-type and p-type MOSFETs operating with the same threshold level have gate-channel leakage current characteristics which are different from each other.

Thus, the inventors discovered that the thickness of the gate oxide film of the p-type MOSFET does not need to be equal to that of the n-type MOSFET. To the contrary, the inventors discovered that the thickness of the gate oxide film of the p-type MOSFET may be thinner than that of the complimentary n-type MOSFET in a single CMOS pair because the

leakage current of the p-type MOSFET is one order of magnitude smaller than that of the n-type MOSFET. Additionally, the thinner gate oxide film of the p-type MOSFET increases the operating speed.

In stark contrast, the Houlihan et al. reference merely discloses the ability to provide different gate oxide thicknesses across a single substrate thereby providing devices which have different properties, while the Campardo et al. reference does not disclose anything at all about gate oxide thicknesses. None of the applied references disclose providing transistors having different gate oxide thicknesses within a single CMOS pair.

The Houlihan et al. reference discloses a method of forming an integrated circuit having four thicknesses of gate oxide in four sets of active areas (Abstract) in a CMOS integrated circuit (col, 1, line 1). The Houlihan et al. reference is concerned with the problem of providing transistors having different characteristics through providing different gate oxide films having different thicknesses. The Houlihan et al. reference explains that conventional methods for providing different gate oxide thicknesses is by providing a resist on areas of gate oxide upon which a thicker gate oxide film is desired and repeatedly etching the remaining areas (col. 1, lines 14-25). The Houlihan et al. reference explains that this method causes problems by creating edge "divots" and planar recess in shallow trench isolation areas (col. 1, lines 21-25).

Houlihan et al. also explains that there is a method for providing several different thicknesses of gate oxide films by using nitrogen implantation (col. 1, lines 26-27). However, Houlihan et al. teaches that this implantation is disadvantageous because the gate thicknesses are dependent upon the nitrogen implant dose and that high dosages can degrade gate oxide film reliability.

Houlihan et al. attempts to address these problems by teaching a method whereby a blanket oxide 20 is formed on active areas (100, 200, 300 and 400). A mask 30 is provided and the blanket oxide 20 in active areas 100 and 400 are exposed to nitrogen implantation (Fig. 2). The reference explains that the nitrogen implantation slows the oxidation process. Next, the mask 30 is removed and an etching mask 40 is formed over active areas 300 and 400. The blanket oxide 20 in active areas 100 and 200 is then etched away through a single HF dip. Lastly, the etching mask 40 is removed and the entire device is thermally oxidized. The resulting device provides gate oxide films with increasing levels of thickness from 100 to 400, respectively.

The Houlihan et al. reference merely discloses varying gate oxide layers between devices to provide logic circuitry with a thin gate oxide for high performance, SRAM array transistors having an intermediate thickness for low leakage and I/O transistors with a thick oxide for resistance to excess voltages (see col. 3, lines 26-32). Therefore, as admitted by the Office action, the Houlihan et al. reference does not disclose a single CMOS pair having MOSFETs with different gate oxide thicknesses.

The Campardo et al. reference does not remedy the deficiencies of the Houlihan et al. reference. Rather, the Campardo et al. reference merely discloses providing a three-well design for a pull down transistor in an output stage of an electronic device. The Campardo et al. does not teach or suggest anything at all about gate oxide thicknesses, let alone a CMOS pair having MOSFETs with different gate oxide thicknesses.

Applicants respectfully request withdrawal of this rejection.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing amendments and remarks, Applicants respectfully submit that claims 1, and 3-20, all the claims presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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CERTIFICATION OF TRANSMISSION

I certify that I transmitted via facsimile to (703) 872-9306 the enclosed Amendment under 37 CFR §1.116 to Examiner Ida M. Soward on February 18, 2004.

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